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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VENT, JAMIE J	

ART UNIT	PAPER NUMBER
2621	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/760,154	TANAKA ET AL.	
	Examiner	Art Unit	
	Jamie Vent	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7, 12, 13, 15-18, and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 12, 13, 15–18, and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Amendment After Final, filed May 3, 2007, with respect to the rejection(s) of claim(s) 1 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sasaki et al (US 5,774,290).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 12, 13, 15 –18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al (US 6,160,673) in further view of Twitchell et al (US 6,281,936) in further view of Sasaki et al (US 5,774,290).

[claims 1 and 22]

Regarding claims 1 and 22 Izumi et al discloses a reproducing apparatus, comprising:

- Reproducing means for reproducing an information signal (Fig. 5. Col. 11 line 38-48);

- Equalizing means for controlling a group delay of the information signal reproduced by said reproducing means (Fig. 5. Col. 11 line 38+);
- Detecting means for detecting a digital signal from the information signal reproduced by said reproducing means (Fig.1 reproduction amplifier 3 as described in Col. 11 line 38-48);
- Control means for controlling a group delay characteristic of said equalizing means by using the reproduced information signal to be inputted to said detecting means and a detection result of said detecting means (Fig. 5. Col. 11 line 38-48); however, fails to disclose a converting means for sampling the information signal output from said equalizing means and for converting the information signal into a digital signal composed of plurality of bits per sample and a detecting means for converting the digital output from said converting means into a n-values signal per sample.

Twitchell et al discloses a transmission system wherein as seen in Figure 1 conversion and equalization of the signal is processed and thereby turns the signal into a digital signal by the A/D converter 80 and further sent to the controller for further processing. Twitchell et al teaches Izumi et al the processing of the signal for converting the signal through the equalizing and converting of the information signal into a digital signal. It is further taught by Sasaki et al the detecting means for conversion of a digital signal as described in Column 3 Lines 50+ through Column 4 Lines 1-30. The digital signal output from the converts the signal and further processes the signal allowing for a proper detection and reproduction of the signal. Therefore, it would be obvious to one

of ordinary skill in the art at the time of the invention to use the reproducing apparatus, as disclosed by Izumi et al, and further incorporating a system that equalizing and converts the signal into a digital signal, as described by Twitchell et al, and further provide a detection means for the converting of the signal based on the sample, as disclosed by Sasaki et al.

[claim 2]

Regarding claim 2, Izumi et al discloses a reproducing apparatus according claim 1, wherein said equalizing means further controls an amplitude of the information signal reproduced by said reproducing means, and said control means further controls an amplitude characteristic of said equalizing means using the reproduced information signal to be inputted to said detecting means and the detection result of said detecting means (Fig. 5. and Fig 6. show the equalizing of the amplitude as further described in column 11 lines 38+ through column 12 lines 1-4).

[claim 3]

Regarding claim 3, Izumi et al discloses a reproducing apparatus according to claim 1, wherein said control means includes multiplying means for multiplying the reproduced information signal to be inputted to said detecting means by the detection result of said detecting means, and an integrating means for integrating a result of multiplication of said multiplying means, and controls the group delay characteristic of said equalizing means according to an output of said integrating means (Fig. 6. and described in Col. 12 line 15-20).

[claim 4]

Regarding claim 4, Izumi et al discloses a reproducing apparatus wherein said multiplying means includes 2n+1 multipliers (n being an integer not less than "2") for respectively multiplying a detection result a predetermined sample and detection results of n samples obtained both before and after the predetermined sample, included in the detection result of said detecting means, by the reproduced information signal corresponding to the detection result of the predetermined sample, and said integrating means includes 2n+1 integrators for respectively integrating outputs said 2n+1 multipliers. (Fig. 6. Col. 12 line 35-56).

[claim 5]

Regarding claim 5, Izumi et al discloses a reproducing apparatus according to claim 4, wherein said equalizing means includes a first group delay control circuit for controlling a group delay of a first predetermined frequency band, and a second group delay control circuit for controlling a group delay of a second predetermined frequency band which is lower than the first predetermined frequency band, and said control means controls a group delay characteristic of said first group delay control circuit according to results of integration of said integrating means of samples obtained n/2 samples before and after the predetermined sample, and controls a group delay characteristic of said second group delay control circuit according to results of integration of said integrating means of samples obtained n samples before and after the predetermined sample (Fig. 7. and described in Col. 13 line 21-28; Col. 5 line 64-Col. 6 line 9; and Col. 9 line 23-49).

[claim 6]

Regarding claim 6, Izumi et al discloses a reproducing apparatus according to claim 5, wherein said control means makes a comparison between results of integration of said integrating means of samples obtained n/2 samples before and after the predetermined sample, and controls group delay characteristic of said first group delay control circuit according to a result of the comparison (Fig. 6.as described in Col. 12 line 47-56; Col. 7 line 51-61; and Col. 8 line 9-16).

[claim 7]

Regarding claim 7, Izumi et al discloses a reproducing apparatus according claim 5, wherein said control means makes a comparison between results of integration of said integrating means of samples obtained n samples before and after the predetermined sample, and controls the group delay characteristic of said second group delay control circuit according to a result of the comparison (Fig. 6. and described in Col. 12 line 35-56).

[claim 12]

Regarding claim 12, Izumi et al discloses a reproducing apparatus according to claim 1 further comprising:

- data detecting means for detecting digital signal composed of one per sample from the reproduced information signal equalized by said equalizing means (Fig.1 reproduction amplifier 3 as described in Col. 11 line 38-48);
- signal processing means for subjecting a predetermined process to an output of said data detecting means (Fig. 5. Col. 11 line 38-48).

[claim 13]

Regarding Claim 13, Izumi et al discloses a reproducing apparatus according claim 12, wherein the information signal includes an image signal as coded, and said signal processing means includes decoding means for decoding the image signal (Column 3 Lines 9-45 describes the decoding of the image signal).

[claim 15]

In regard to Claim 15, Izumi et al discloses a reproducing according claim wherein the information signal a PR4-precoded signal and said detecting means includes a decoder for PR4-decoding information signal equalized by said equalizing means, and detects a digital signal from the information signal outputted from said decoder (Column 4 Lines 9-45 describes the precoded and decoding signal for detecting the digital signal).

[claim 16]

Regarding claim 16, Izumi et al discloses a reproducing apparatus, comprising:

- Reproducing means for reproducing an information signal (Fig. 5. Col. 11 line 38-48);
- Equalizing means for equalizing the information signal reproduced by said reproducing means (Fig. 5. Col. 11 line 38-48. Col 19 line 6-11);
- Control means for controlling an equalizing characteristic of said equalizing means, said control means having a first mode of controlling the equalizing characteristic by using first control method, and a second mode of controlling the equalizing characteristic by using a second control method (Fig. 5. Col. 11 line 38-48. Fig. 6. Col 16 line 8-18).

[claim 17]

Regarding claim 17, Izumi et al discloses a reproducing apparatus according to claim 16, wherein said control means changes over the first mode and the second mode according to elapsed time (Col. 19 line 12-20).

[claim 18]

Regarding Claim 18, Izumi et al discloses a reproducing apparatus according to claim 16, wherein said reproducing means reproduces the information signal from a recording medium having a number of helical tracks formed thereon, and said control means changes over the first mode and the second mode according to the number of reproduced tracks of the recording medium (Column 2 Lines 8-67 describes the video tape recorder which thereby has helical track).

3. Claims 8,9, and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al (US 6,160,673) in further view of Twitchell et al (US 6,281,936) in further view of Sasaki et al (US 5,774,290) in view of Williams (US 6,344,749).

[claim 8]

In regard to Claim 8, Izumi et al discloses a reproducing apparatus according to claim 1, wherein said equalizing means (Fig. 5. Col. 11 line 38+); however, fails to disclose that the equalizing means includes a first group delay equalizing circuit for controlling a group delay of first predetermined frequency band, and a second group delay equalizing circuit for controlling a group delay of a second predetermined frequency band which lower than the first predetermined frequency band, and said control means controls a

group delay characteristic said first group delay equalizing circuit and a group delay characteristic of said second group delay equalizing circuit independently of each other. Williams discloses a system wherein Column 2 lines 13-25 wherein group delay provides varying group delays. The circuit containing various filters and circuits allow for the system to having various delays and thereby providing a system with little distortion. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the reproducing apparatus, as disclosed by Izumi et al, and further incorporate a system which uses delays through the use of filters for equalizing the circuit, as disclosed by Williams.

[claims 9 & 11]

In regard to Claims 9 and 11, Izumi et al discloses a reproducing apparatus; however fails to disclose according wherein each of said first group delay equalizing circuit and said second group delay equalizing circuit includes an all-pass filter and an FIR (finite impulse response) filter for filtering an output of an equalizing means. Williams discloses a system wherein the first group delay provides an all-pass filter through the combination of filters as shown in Figure 10 and described in Column 16 Lines 40+. The use of filters provides the system for proper filtering of the signal and to further provide equalization of the signal through the system. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the reproducing apparatus, as disclosed by Izumi et al, and further incorporate a system wherein various filters are used to output to the equalizing means of the system, as disclosed by Williams.

4. Claims 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al (US 6,160,673) in further view of Twitchell et al (US 6,281,936) in further view of Sasaki et al (US 5,774,290) in further view of Limberg et al (US 6,426,780).

[claim 14]

Regarding Claim 14, Izumi et al discloses a reproducing apparatus according claim 12, however, fails to disclose the data detecting means detects the digital signal composed of one per sample by using a Viterbi algorithm. Limberg et al discloses the detecting the digital signal is done through Viterbi algorithm as described in Column 7 Lines 18-40. Through using the Viterbi algorithm allows for recognition of patterns of the digital signal thereby allowing for more efficient recognition of the signal. . Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the reproducing apparatus, as disclosed by Izumi et al, and further incorporate a system wherein the Viterbu algorithm is used for detecting digital signal, as disclosed by Limberg et al.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamie Vent whose telephone number is 571-272-7384. The examiner can normally be reached on 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on 571-272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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